Nishimura does not disclose the combination of features recited in claims 1 and 13 (the following claim recitations are taken from claim 1 for convenience). For example, Nishimura lacks "a multi-bit wide system bus, coupled to said circuit and said memory, for transferring multi-bit data words between said circuit and said memory in response to memory transfer requests issued upon said system bus during normal processing operation of said circuit and said memory." Thus, the same system bus is used both for memory transfer requests during normal processing operation and for issuing memory write requests in response to a state saving trigger.

On page 4 of the Office Action, the Examiner asserts that the 16 and 64 bit buses described in Nishimura's column 8, lines 22-30 correspond to the claimed multi-bit wide system bus. Applicants disagree. These lines describe "the system bus SYSBUS [that is] made up of the 16-bit address bus ABUS and the 16-bit data bus DBUS" and "the 64-bit data bus SDBUS." But none of these buses is used both for normal processing operation of the circuit and for transferring a sequence of memory write requests in response to a state saving trigger. Column 7, lines 18-25 explains that: "the CPU core has two data routes, i.e. the system bus SYSBUS and exclusive-use data bus SDBUS. The system bus SYSBUS is used for passing normal addresses and data, ..., and the data bus SDBUS for **exclusively** passing data saved from or restored to the register set RF, program counter PC, and processor status word PSW." (Emphasis added). Thus, in Nishimura, the 64-bit SDBUS is used **exclusively** for passing data saved from or restored to the register set, and the 16-bit SYSBUS is used for passing addresses and data during normal processing operation of the circuit). This is further emphasized in column 8, lines 31-39:

> When the on-chip RAM 3 is normally used as a main memory, data in the memory is accessed in a unit of 16 bits at relatively low speed through the system bus SYSBUS according to bus access rules. When the CPU core 2 switches one register bank to another to save or restore data from or to the register set, data is transferred

> in a unit of 64 bits at high speed through the exclusive-use data bus SDBUS according to an address provided through the bank address bus.

Because Nishimura teaches two separate buses—one for use during normal processing and the other for state saving, Nishimura does not disclose the combination of the claimed multi-bit wide system bus .

Nishimura also fails to disclose the claimed state saving controller: "a state saving controller, coupled to said circuit and said system bus, configured in response to a state saving trigger to read said data values defining a state of said circuit from said one or more nodes and to generate a sequence of memory write requests on said system bus that write one or more state saving multi-bit data words representing said data values into said memory...." The Examiner identifies control 27 in Figure 5 and column 7, lines 52-55 of Nishimura. Column 7, lines 51-52 state that "Figure 5 shows the inside of the general purpose register set RF disposed in the CPU core." Thus, the read-write controller 27 is an internal controller that is part of the register set RF. But where does Nishimura disclose that the internal register set's read-write controller 27 is "configured in response to a state saving trigger to read said data values defining a state of said circuit from said one or more nodes and to generate a sequence of memory write requests on said system bus that write one or more state saving multi-bit data words representing said data values into said memory such that said state of said circuit is restorable using said one or more state saving multi-bit data words"? Figure 5 simply shows a BNKTX command the indicates "that data is transferred from register file to bank RAM" via the separate and exclusive-use data bus SDBUS. Again, the exclusive-use data bus SDBUS is not Nishimura's system bus SYSBUS. The only section of Nishimura that describes controller 27 is column 7, line 53 to column 8, line 9. These lines describe a "selected address" being provided to the controller 27 by various

components of Figure 5. No further functions are described for the controller 27. So Nishimura's controller 27 does not disclose the claimed state saving controller generating a sequence of memory write requests on the system bus SYSBUS.

Lacking multiple features recited in the claims, the anticipation rejection is improper and should be withdrawn.

Most of the claims stand rejected for obviousness under 35 U.S.C. §103 based on Godfrey in view of Nishimura. This rejection is respectfully traversed.

Applicants first address the Examiner response to arguments set forth in the Appeal Brief. The Examiner rejects the distinction that Godfrey's system bus 100 is not coupled to the memory 200 (it is assumed the Examiner means 200 and not 100). The Examiner contends that "[t]he SCAN_PATH is part of the system bus 100," and in support, the Examiner quotes col. 4, line 65 to col. 5, line 6 of Godfrey. But this text do not support the Examiner's assertion. The quoted lines state that "the configuration scan data from each peripheral device is sequentially shifted out of each configuration register into external memory 200 via SCAN_PATH. Likewise, the external memory 200 is coupled to the input pin IN, so that configuration scan data from external memory 200 can be synchronously shifted into each peripheral configuration register via SCAN_PATH." Nothing in these lines states that the SCAN_PATH is part of the system bus 100. In fact, the system bus 100 is not even mentioned here. Figure 2 shows that the system bus 100 (the boldest lines connecting the peripheral devices in Figure 2) is entirely separate from the SCAN_PATH (the second boldest lines connecting the peripheral devices) and is not part of the SCAN_PATH. Figure 2 also makes clear that the system bus 100 is not coupled to the memory 200. Thus, the Examiner's assertion is unfounded.

The Examiner also argues: "It's clearly, as mentioned above that the configuration data is shifted in and out between the entire bus 100 and SCAN_PATH." But the passage quoted by the Examiner states that configuration scan data is shifted out of each configuration register into external memory and into each configuration register from external memory via the SCAN_PATH. Thus, it is incorrect to say that data is shifted in and out between the bus 100 and the SCAN_PATH.

Page 3 of the Office Action asserts that "each configuration register as a result of the JTAG self test/diagnosis must have a path which is connected to the external memory so that the scan data of each register can be saved into external memory, or the configuration data can be loaded into each register from the external memory as taught by Godfrey... If the bus 100 of Godfrey is not connected to memory 200, then the save/restore operation of Godfrey's system is meaningless" (emphasis added). Applicants disagree. Godfrey discloses that "the configuration registers of clock and power management unit 102 ...[Godfrey lists the peripheral devices shown in Figure 2] ... are daisy chained (i.e. serially connected) together via signal line SCAN_PATH", "the SCAN_PATH line ... is coupled to the output pin OUT of the microcontroller M" and "the out pin OUT is coupled to an external memory 200" (col. 4, lines 54-67) (emphasis added). The plain language of this quoted text makes clear that Godfrey does provide a path connecting the configuration registers and the external memory—the SCAN_PATH signal line (via the output pin OUT). Note that col. 4, line 65 to col. 5, line 6 do not even mention the system bus 100. And contrary to the Examiner's assertion, it is not necessary for the bus 100 to be connected to the memory in order for the save/restore operation of Godfrey to have meaning. Godfrey sequentially shifts data between the configuration registers and external memory using the

SCAN_PATH, independent of the operation of the system bus 100. The save and restore operation of Godfrey does not require the system bus 100 to be connected to the memory.

Also, the Examiner asserts that "Godfrey further teaches [**the scan path is in accordance with IEEE 1149.1 bus standard**]" (emphasis in original) to justify the assertion that the bus and SCAN_PATH are connected. But the fact that the scan path is in accordance with the IEEE 1149.1 bus standard does not prove that the bus 100 is part of the SCAN_PATH or connected to the SCAN_PATH, or that the bus 100 is connected to the memory.

Turning now to the rejection based on Godfrey in combination with Nishimura, the Examiner cites column 5, lines 8-10 and 27-35 in Godfrey as disclosing the system bus. But these lines do not mention the system bus 100 and certainly do not teach that bus coupled to the memory 200. Also, claim 1 recites a system bus "for transferring multi-bit data words between said circuit and said memory in response to memory transfer requests issued upon said system bus during normal processing operation of said circuit and said memory." Where does Godrey describe using the external memory 200 during normal processing operations?

Godfrey also does not disclose "a state saving controller, coupled to said circuit and said system bus, configured in response to a state saving trigger to read said data values defining a state of said circuit from said one or more nodes and to generate a sequence of memory write requests on said system bus that write one or more state saving multi-bit data words representing said data values into said memory such that said state of said circuit is restorable using said one or more state saving multi-bit words." Godfrey does not generate a sequence of memory write requests on the system bus 100 in response to a state saving trigger. Instead, a separate signal line (SCAN_PATH) is used to shift configuration data into memory in response to a trigger. That data transfer across the SCAN_PATH is as a serial data signal (see col. 7, lines 51-52). As

a result and as admitted by the Examiner, Godfrey does not disclose writing one or more state saving multi-bit data words into memory, and thus, Godfrey does not disclose the claimed state saving controller.

As explained above, Nishimura also does not disclose the features missing from Godfrey. Again, Nishimura requires two totally separate data buses: one (SYSBUS) for normal data processing operations and the other (SDBUS) for exclusive use to save/restore register/state data. Neither Godfrey nor Nishimura disclose using the same multi-bit wide system bus both for transferring multi-bit data words in response to memory transfer requests issued on the bus during normal processing operations of the circuit and memory, and for having write requests generated on the bus that write one or more state saving multi-bit data words to memory in response to a state saving trigger. In Godfrey, a SCAN_PATH that is separate to the internal bus is provided for shifting configuration data between configuration registers and external memory. Thus, both references require a system bus and an additional data path for handling saving state data. Neither reuses the system bus and memory which are already provided in a processor or provides such simple state saving controller that achieves rapid, efficient, and complete saving and later restoring of system state.

The application is in condition for allowance. An early notice to that effect is requested.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: _____
John R. Lastova
Reg. No. 33,149

JRL:maa
901 North Glebe Road, 11th Floor
Arlington, VA 22203-1808
Telephone: (703) 816-4000
Facsimile: (703) 816-4100